REMARKS

The Examiner's Office Action mailed on December 5, 2003 has been received and its contents carefully considered.

Claims 1-8 are pending in this application and are amended herein. Claim 4 is rewritten in independent form, incorporating the limitations of claim 1, to make it clearer that it is directed to the second exemplary embodiment of switching control equipment illustrated in Figure 6. Thus, as amended, claims 1, 4 and 5 are independent claims.

In the Action, the Examiner has objected to the drawings because reference character "120b" (Figure 2) has been used to designate both the switching correspondence unit and the network switching controller. To avoid any possible confusion, the reference designation for the switching correspondence unit has been changed to "120c" in both Figure 2 and Figure 6, and in the related text of the specification. In addition, the applicants have noted and corrected spelling errors in boxes and 12a and 124b in Figures 1, 2 and 6. The Examiner's review and approval of the corrected drawings attached to this Amendment as Appendix 2 are respectfully requested.

The Examiner has also objected to the abstract is being excessive in length, and to the specification in general as being "replete with terms which are not clear, concise and exact." Specifically, the Examiner points to the discussion of the right/read enable signals and write/read signals on page 14, as not being understandable, and to the description on page 7 in the Summary of the Invention, as being unclear. The objections raised by the Examiner, as well as other possibly unclear language identified by the applicants in reviewing the application, have been addressed in the amended specification and abstract attached to this Amendment as Appendix 1. No new matter has been added by the changes to the specification. The Examiner's review and approval of the amended specification and abstract are respectfully requested.

In the Action, claims 1-8 are rejected under 35 USC §112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. The Examiner asserts that the claims are generally narrative and indefinite, failing to conform with current U.S.

practice. The Examiner cites several examples in claims 1, 4 and 5. These and other deficiencies in the claim language are addressed in the amendments to the claims made herein. The Examiner's entry of the amended claims and withdrawal of the §112, second paragraph, rejection are respectfully requested.

Claims 1-8 also stand rejected under 35 U.S.C. §103(a) is being obvious over Suzuki (U.S. Patent No. 4,759,012) in view of Ohtawa (U.S. Patent No. 5,130,979). Claims 1-8 are amended herein to more clearly distinguish the present invention over the applied references.

With regard to claim 1, the Examiner points to Suzuki as teaching multiplexing means 20 for multiplexing time slots from a plurality of circuits; switching memory means 6 for storing and switching data of the time slots supplied from the multiplexing means, for one frame portion (column 4, lines 63-64); switching control means 22 comprising switching correspondence means 22 for directing interchange of the time slots of the switching memory means in response to a switching request from an upper layer controller 12; demultiplexing means 21 for demultiplexing as read out using data supplied from the switching correspondence means as addresses of the switching memory means into the plurality of circuits, the switching correspondence means further comprising: information receiving means 10 for receiving connection information from the upper layer controller; read-out regulating means 10 for writing the writing the connection information received through the information receiving means to an address designated by the connection information, in a first memory means 11 and a second memory means 11; and read-out selection means 19 for selecting read-out from either the first memory means or the second memory means of the same.

The applicants disagree. Claim 1, as amended, requires that the read-out selection means select read-out from one of the first memory means and the second memory means "in response to the switching signal provided by the network switching control means." The switching signal is, in turn, generated "in response to a "switching request provided by the upper layer controller." Thus, in the claimed invention, the selection of a memory means by the read-out selection means is not changed unless and until a switching request is received from the network.

By contrast, controlling of the write-in/read-out at the time switch 6 of the

apparatus in Suzuki is conducted alternately by the channel transfer memories 11_1 and 11_2 for each frame. While the channel transfer memory 11_1, for example, is controlling the write-in/read-out of the time switch 6, the time switch control data for the next frame is set at the other channel transfer memory 11_2 (column 4, lines 19-25). Thus, in Suzuki, the selection of a memory means by the read-out selection means is performed for each frame and not simply when a switching request is received from the network.

Further, the Examiner acknowledges that Suzuki fails to teach the network switching control means for generating a switching signal. To cure this defect in the base reference, the Examiner points to Ohtawa as teaching a network switching control means 11 for generating a switching signal (column 2, lines 40-41), and argues that it would have been obvious to one skilled in the art to modify Suzuki to include the network switching means for generating a switching signal as taught by Ohtawa in order to achieve efficiency through synchronization.

The applicants respectfully disagree. Ohtawa is directed to a frame converter using a dual-port random access memory, which does not itself perform any switching functions. The text referenced by Examiner discloses only that the call processor 11 supplies a space switching signal to the space switch 17 to cause it to selectively couple the TDMA inputs from memories 15a and 15b to the inputs of time division demultiplexers 18a and 18b whose outputs are respectively coupled to the subscriber lines A1 to A16 and B1 to B16. The referenced text fails to disclose that the call processor generates a switching signal in response to a switching request provided by the network, to be used in selecting address data for reading time slot data stored in dual-port random access memories 15a and 15b. Hence, it is respectfully submitted that Ohtawa lacks any teaching or suggestion that would motivate one of ordinary skill in the art to make the combination proposed by the Examiner. It appears that the Examiner has in hindsight taken an individual element out of the Ohtawa reference without proper consideration of what the reference teaches as a whole.

For at least the reasons discussed above, it is respectfully submitted that claim 1, as well as claims 2-8, patentable distinguish over the applied references, whether considered individually or in combination.

In summary, it is submitted that this Amendment places the application in condition for allowance. Notice of allowance and passing of this application to issue are respectfully requested.

Should the Examiner feel that a conference would help to expedite the prosecution of this application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such an interview.

Respectfully submitted,

May 5, 2004
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Appendix 1 - Amended Specification and Abstract (24 pgs)

Appendix 2 - Replacement Drawing Sheets (4)

ABSTRACT OF THE DISCLOSURE

~~A digital switching system comprises multiplexing means for multiplexing time slots from a plurality of circuits, multiplexed respectively, by the multiplexed time slot unit, switching memory means for storing and switching data of the time slots supplied from the multiplexing means, for one frame portion, switching control means comprising switching correspondence means for directing interchange of the time slots of the switching memory means in response to a switching request from an upper layer controller, and demultiplexing means for demultiplexing data as read out using data supplied from the switching correspondence means as addresses of the switching memory means into the plurality of the circuits, the switching correspondence means further comprising information receiving means for receiving connection information from the upper,, layer controller, read out regulating means for writing the connection information received through the information receiving means to an address designated by the connection information, in a first memory means and a second memory means, respectively, for storing the connection information corresponding to before or after switching, and sequentially reading out the connection information stored, in read out order of the switching memory means, network switching control means for generating a switching signal in synchronization with an internal standard timing in response to a switching directive of a network, delivered from the upper layer controller, and read out selection means for selecting read out from either the first memory means of the read out regulating means or the second memory means of the same in response to the switching signal delivered from the network switching control means.~~